

WHAT IS CLAIMED IS:

1           1.    A   Content   Addressable   Memory   ("CAM")  
2    architecture providing improved speed, comprising:  
3       -    an array of CAM cells connected to a compare-  
4            data-write-driver and to a read/write block,  
5            for receiving the compare-data and for reading  
6            and/or writing data in the array of CAM cells  
7            respectively,  
8       -    outputs of the said CAM cell are coupled to a  
9            match block providing match outputs signal  
10           lines that identifies a match/no-match at the  
11           end of a search operation, and;  
12       -    a control logic for implementing search and  
13            address decoding operations during first state  
14            and enabling read-or-write operations within  
15            the second state of the same clock cycle in the  
16            event of a match.

1           2.    The CAM architecture as claimed in claim 1,  
2    wherein the control logic comprising a sequencing circuit  
3    that enables the data comparators of the CAM cell array  
4    and the address decoder of read/write block during the  
5    first state of the clock and enables the read-or-write  
6    operation in the second state of the same clock.

- 1           3.   A method for improving speed of a Content  
2   Addressable Memory ("CAM") architecture in steps of:
- 3           -   connecting an array of CAM cells to a compare-  
4               data-write-driver and to a read/write block,  
5               for receiving the compare-data and for reading  
6               and writing data in the CAM cell respectively,
  - 7           -   coupling a match block to said array of CAM  
8               cell providing match outputs signal lines for  
9               identifying a match/no-match at the end of a  
10              Search operation,
  - 11          -   performing the search and address decoding  
12               operations during first state of the clock  
13               cycle, and;
  - 14          -   implementing the read/write operation after a  
15               successful search during the second state of  
16               the same clock cycle.